Ram Srivatsa Kannan

Software Engineer / Systems Researcher

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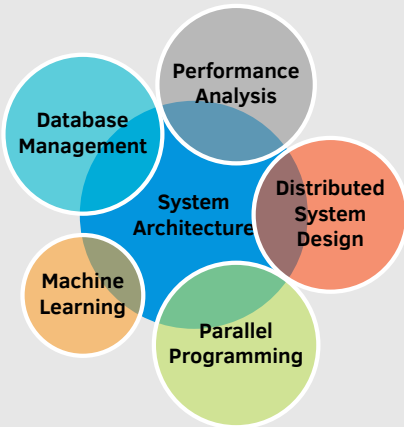🌐 https://ramsrivatsa.github.io

✉ ramsri@umich.edu

in/ramsrivatsa

ramsrivatsa

Skills

Overview

Programming

Golang

Verilog • VDHL

Python • Bash

C • C++

Hive • SQL

Java

Education

Aug 2013 - Dec 2018	**Ph.D. Computer Science** Ann Arbor, Michigan, USA *Thesis: Enabling Fairness in Cloud Computing Infrastructures*	University of Michigan
Aug 2009 - April 2013	**B.Tech Information Technology** Madras, Tamil Nadu, India Thesis: SCOC IP design for Application Specific Architectures	MIT, Anna University

Experience

August 2020 - Present — **Software Engineer** — *Yugabyte*

- **Yugabyte DB** Part of a team that builds strongly consistent distributed databases.

March 2019 – August 2020 — **Software Engineer** — *Uber Technologies*

- **Shadow: Safe Rollout System** Designing a distrubuted system for automated safe roll out of microservices in Uber. Pursuing research on automating integration tests for services as a part of safe rollout pipeline.
- **SubmitQueue: Keeping Master Green at Scale** Optimizing SubmitQueue, a distributed system for for maintaining a green masters in a monorepo.

Fall 2013 – Fall 2018 — **Graduate Research Assistant** — University of Michigan, Ann Arbor

- **Proctor: Identifying Interference in Shared datacenters** - Designed a real-time technique for identifying problematic VMs and its root causes in hyper-converged datacenters that executes CPU, Network and I/O intensive applications.
- **Caliper: Interference Estimator for Multi-tenant Environments Sharing Architectural Resources** - Designed a runtime system to estimate performance degradation of applications running in public clouds and to price users accordingly.
- **GrandSLAm – Guaranteeing Datacenter SLAs for Microservices executing in Serverless Computing Infrastructures** - Designed a runtime system to guarantee SLAs among applications utilizing microservers in a serverless computing platform. Implemented DNN based machine learning algorithms in serverless framework using tensorflow on docker containers for this purposes.
- Architecture design for data migration of media files from application to Azure cloud.
- **Big Data analytics on GPUs** - Implemented parallel versions of common data analytics queries and compared it with parallel pthreads versions of the queries in terms of performance. Performed a characterization study of how different input formats of data would affect the performance of queries.
- **Prophet: Precise QoS Prediction on Non-Preemptive Accelerators to Improve Utilization in Warehouse Scale Computers** - Collaborated towards building a GPU based datacenter which gurantees Quality-of-Service for latency-sensitive applications for the state of the art web service applications.
- **Tail-Sniping: Tail Latency Troubleshooting Using Causal Inference** - Collaborated towards building a runtime system to detect performance anomalies using microarchitectural resources and to perform causal analysis with them.

Courses

Systems
Computer Architecture
Advanced Compilers
Parallel Architectures
Microarchitecture
Operating Systems

PL
Data Structures
Algorithms
Embedded Systems
OOP

Misc
Artificial Intelligence
Probability
Statistics

Interests

Datacenter Design

Cloud Computing

Distributes Systems & OS

Software Development

Computer Architecture

Tools

TensorFlow Keras Pandas Numpy Lucida

Matplotlib Excel gnuplot Plotly LaTeX

MySql Elastic-Search Hadoop Spark Storm

perfmon esxtop io-analyzer netperf

git tmux AWS kvm esxi linux unix

Hobbies

Summer '18 **Research Intern – VMware Research** VMware Inc.
Worked on a compiler infrastructure that optimizes the compilation times of Verilog in FPGA. Worked on a real time static compiler/scheduler that schedules independent modules present in a Verilog codebase in an optimal order such that emulation time is reduced.

Summer '16 **Research Intern – Performance Engineering** VMware Inc.
Worked on real-time, scalable analytics platform which we could automatically detect antagonistic VM behaviors in co-located environments caused due to disk contention using real time system telemetry. Using our technique we were able to identify performance issues and increase individual VM performance by up to $2.5\times$ and $1.8\times$, on an average.

Winter '18
Fall '16, '15 **Graduate Student Instructor** University of Michigan
- EECS 483 – Compiler Construction
- EECS 280 – Programming and Data Structures
- EECS 583 – Advanced Compilers

Fall '10 –
Summer '13 **Research Trainee** Waran Research Foundation (WARFT), India
- Worked in the high performance computer architecture group that is focused in designing CUstom Built hEterogeneous Multi-coreArCHitecture - CUBEMACH a node architecture for future generation supercomputing clusters

publications

- **Caliper: Interference Estimator for Multi-tenant Environments Sharing Architectural Resource**, Ram Srivatsa Kannan, Michael Laurenzano, Jeongseob Ahn, Jason Mars, Lingjia Tang, ACM Transactions on Architecture and Code Optimization (ACM TACO 2019)

- **GrandSLAm - Guaranteeing SLAs for Microservices executing in Serverless Computing Infrastructures**, Ram Srivatsa Kannan, Lavanya Subramanian, Ashwin Raju, Jeongseob Ahn, Jason Mars, Lingjia Tang, European Conference on Computer Systems (Eurosys-19), March 2019

- **Prophet: Precise QoS Prediction on Non-Preemptive Accelerators to Improve Utilization in Warehouse Scale Computers**, Quan Chen, Hailong Yang, Minyi Guo, Ram Srivatsa Kannan, Jason Mars, Lingjia Tang, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-17), April 2017

- **Proctor: Identifying Interference in Shared datacenters**, Ram Srivatsa Kannan, Animesh Jain, Michael Laurenzano, Jason Mars, Lingjia Tang, International Symposium on Performance Analysis of Systems and Software (ISPASS-18), April 2018

- **Compilation Accelerator on Silicon**, Venkateswaran Nagarajan, Ram Srivatsa Kannan et.al., published in the proceedings of 11th IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2012, University of Massachusetts, Amherst

- **SCOC IP Cores for Custom Built Supercomputing Nodes**, Venkateswaran Nagarajan, Ram Srivatsa Kannan et.al., published in the proceedings of 11th IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2012, University of Massachusetts, Amherst

professional activities

Reviewer **Conferences**
OSDI 2020 (Artifact Evaluation Committee), SRDS 2020, InfoComp 2020 (Program Committee), CCGrid 2020, ISCA 2019, PLDI 2018, MICRO 2018, ISCA 2016, HPCA 2016, ASPLOS 2016